REMARKS/ARGUMENTS

Claims 1-20 remain pending in this application and stand rejected. Claims 1, 2, 11, and 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent Publication 2004/0216005 ("Pramanick") in view of U.S. Patent Publication 2002/0030683 ("Alexander") and further in view of U.S. Patent No. 6,898,771 ("Tojima"). Claims 3-10 and 13-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Pramanick in view of Alexander, and further in view of Tojima, as applied to claims 1 and 11, and further in view of U.S. Patent No. 6,662,126 (Liu). Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over Pramanick in view of Alexander, and further in view of Tojima, as applied to claims 1 and 11, and further in view of U.S. Patent No. 6,466,898 (Chan).

Applicant traverses these rejections for at least the reasons cited below. Nonetheless, to expedite the prosecution of the instant application, Applicant has amended claims 1 and 11 to clarify their respective languages and further define the scope of the present invention. For example, claim 1 is amended to recite, in part, "selecting first and second signals applied to nodes internal to the circuit based on input received from a user". Support for this limitation is provided throughout the original disclosure. For example, paragraphs 5 of the original disclosure provides:

"All references herein to circuit simulation tools, or timing analysis tools, should be understood to include all tools that perform verification of the circuit design, by either, dynamic simulation of signal levels at all nets in the list, or static computation of propagation delays traversing paths on the netlist. This applies to verification tools and techniques used as part of netlist optimization, synthesis, placement and routing EDA tools in the overall EDA design processing flow.

Pramanick is directed at debugging failures of an integrated circuit (IC) device that has already been designed. In contrast, the present invention is directed at using an EDA tool

to simulate and verify a circuit during the design phase. For example, claim 1 recites, in part, "...to simulate the circuit".

Pramanick states in the Abstract:

"A test method for debugging failures of an IC device with use of an event based semiconductor test system is capable of distinguishing a timing related failure from other failures. The test method includes the steps of: applying a test signal to a DUT...." (Abstract)

In other words, Pramanick is only concerned with signals that are applied/received by input/output ports of an IC device. There is no disclosure, not even a mention, in Pramanick of "....nodes internal to the circuit based on input received from a user... to simulate the circuit." as recited, in part, in claim 1.

In rejecting claims 1, 2, 11 and 12, the examiner also refers to paragraphs 48-50 of Pramanick. In paragraphs 48-50 Pramanick states:

"FIG. 6 also shows an overall relationship between the event based test system and an EDA (electronic design automation) environment although the EDA environment itself is not directly related to the subject matter of the present invention. Because the data structure in the event based test system is in the event format, the EDA environment and the test system can be interrelated in a seamless fashion."

As best understood, the above excerpts of Pramanick suggests taking the EDA data in order to provide input stimulus for input ports and generate the expected results at the output ports. Pramanick is completely silent on using EDA tools to simulate a circuit to perform analysis of internal nodes during the design phase of the circuit. In fact, Pramanick states:

"the EDA environment itself is not directly related to the subject matter of the present invention" (paragraph 48)

Pramanick, whether taken alone or in combination with Alexander and Tojima, fails to teach or suggest claim 1 for at least the above reasons. Claims 2-10 are dependent from claim 1 and are thus allowable for at least the same reasons as is claim 1. Claim 11 and its dependent claims 12-20 are also allowable for at least the same reasons as is claim 1.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 752-2424.

Respectfully submitted,

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